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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/626,634	07/25/2003	An-Ru Andrew Cheng	TOP 298	9620

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EXAMINER	
LEVIN, NAUM B	

ART UNIT	PAPER NUMBER
2825	

DATE MAILED: 04/15/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/626,634	CHENG ET AL.	
	Examiner	Art Unit	
	Naum B. Levin	2825	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *25 July 2003*.

2a)☐ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-13* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-13* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *25 July 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

1. Claims 1-10 are rejected under 35 U.S.C. 102(e) as being unpatentable by Balachandran et al. (US Patent 6,618,830).

As to claim 1 Balachandran discloses:

An integrated circuit on a chip, comprising:

a substrate (col.1, ll.14-15); and

at least one scan chain disposed in the substrate (wafer), with scan cells connected to form a series chain, each connection being formed according to a layout constraint with a minimum dimension provided by design rules for an assigned routing layer (col.1, ll.14-47; col.1, ll.52-61; col.6, ll.15-30; col.6, ll.50-63).

As to claims 2-10 Balachandran describes:

(2) The integrated circuit as claimed in claim wherein the assigned routing layer is a first metal layer (col.6, ll.50-63);

(3) The integrated circuit as claimed in claim wherein the layout constraint limits the connection to passage through at least the first metal layer (col.4, ll.7-37; col.6, ll.15-30; col.6, ll.50-63);

(4) The integrated circuit as claimed claim wherein the layout constraint limits the connection to passage through only the first metal layer (col.4, ll.7-37);

(5) The integrated circuit as claimed in claim wherein the layout constraint limits each metal line of the first metal layer, to form the connection, to line width of critical dimension (CD) of the first metal layer (col.6, ll.15-30);

(6), (10) The integrated circuit as claimed in claim wherein the layout constraint further limits any metal line of a second metal layer in the connection to a line width exceeding CD of the second metal layer (col.8, ll.24-55);

(7)-(9) The integrated circuit, wherein the layout constraint further requires any plug (metal lead) of a plug layer linking two metal lines in the connection to be more than one (col.1, ll.52-61; col.6, ll.50-63).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 11-13 are rejected under 35 U.S.C. 103(a) as being unpatentable over Balachandran in view of Barth et al. (US Patent 6,233,184).

With respect to claims 11-13 Balachandran teaches the features above but lacks

an integrated circuit on a chip further comprising an auxiliary routing net positioned in parallel beside the scan chain to replace one of the connections in the scan chain, and the auxiliary routing net does not function when the scan chain is originally formed.

As to claims 11-13 Barth recites:

The integrated circuit, wherein the integrated circuit further has an auxiliary routing net (membrane ribbon connectors 31) positioned in parallel beside the scan chain, the auxiliary routing net has metal lines of different lengths to replace one of the connections in the scan chain, and the auxiliary routing net does not function when the scan chain is originally formed (col.1, ll.5-10; col.4, ll.42-64; col.8, ll.19-67; col.9, ll.1-6; col.12, ll.48-65).

It would have been obvious to a person of ordinary skills in the art at the time the invention was made to employ Barth's teaching regarding the integrated circuit on a chip further comprising an auxiliary routing net positioned in parallel beside the scan chain to replace one of the connections in the scan chain, and the auxiliary routing net does not function when the scan chain is originally formed and use it in Balachandran's invention to replace failing cells, word lines or bit lines by disconnecting shorted cells and connecting good cells into chains, thereby improving wafer burn-in scheme that permits parallel test and burn-in of the chips on a wafer before dicing without a costly glass ceramic interface.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Naum B. Levin whose telephone number is 571-272-1898. The examiner can normally be reached on M-F (8:00-4:30).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matthew S. Smith can be reached on 571-272-1907. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Naum Levin
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